AMENDMENTS IN MARK-UP FORM

The changes made by the above amendments are shown here in mark-up form.

The last paragraph on page 11 is amended as follows:

Coverage measurement module 334 processes a pattern profile 322 using a set of coverage parameters 324 to produce a set of analysis results 318. Coverage measurement module [324]334 preferably determines a coverage measurement according to the extended DVG method described above, although other coverage measurements may be used. The coverage parameters 324 may specify the criteria being used to determine coverage, including categorization rules and desired levels of coverage when the extended DVG method is used. The measurement results 318 may be processed by the profile generation module 330 to determine profiles of new test patterns or modified test patterns designed to improve the measured coverage.

The abstract is amended as follows:

A profile-based system is described for verifying the functionality of a device design. In one embodiment, the system includes a profile generation module, a coverage measurement module, and a pattern generation module. The profile generation module operates from a rule set that represents the design specification and any applicable standards, and a profile mode that specifies "interesting" aspects of test patterns for device design verification. [The interesting aspects are determined by the user and may be somewhat subjective, although it is preferable that the aspects relate to the coverage provided by the test pattern. Given the rule set and the profile mode, the]The profile generation module determines an ordered set of variable values that [at least partially] specify a test pattern, and produces a profile that intelligibly describes the interesting aspects of the test pattern. [Tools such as the coverage measurement module and the pattern generation module may then operate on the profile of the test pattern.] The coverage measurement module analyzes the profile to determine coverage, and the analysis results may be operated on by the profile generation module to determine a profile for an improved test pattern. [The coverage measurement module may preferably employ a design-vector grading (DVG) metric or a variation thereof.] The pattern generation module converts the profile into a test pattern having the interesting aspects specified in the profile. [The system may further include a pattern profiling module for converting existing test patterns into profiles, and a pattern checking

module for verifying that profile-represented patterns satisfy particular rules. This system efficiently produces test patterns that are better understood by the user and that enable better coverage to be achieved.]

REMARKS

Based on the above amendments and the following remarks, applicants respectfully submit that all the pending claims are in condition for allowance.

Status of the Claims

Claims 1-20 remain pending.

Objections to the Specification

The examiner objected to the abstract for exceeding 150 words. Applicants have amended the specification accordingly.

The examiner further noted informalities in the specification. Applicants have amended the specification to correct the noted errors.

Rejections Under 35 USC § 102 and § 103

The examiner rejected claims 1-5, 11-13 and 17-19 under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,949,691 ("Kurosaka"). The examiner further rejected claims 6-10, 14-16 and 20 as being unpatentable over various combinations of Kurosaka and U.S. Patent No. 6,141,630 ("McNamara") and U.S. Patent No. 5,684,808 ("Valind"). Applicants respectfully traverse these rejections.

To establish a rejection under 102 or 103, the examiner must show that the cited references teach or suggest every element of the claims. (*See, e.g.,* MPEP 2131, 2142).

Claim 1 recites in part: "a pattern profile that represents a test pattern, wherein the pattern profile includes a human-intelligible description of aspects of the test pattern". On lines 16-22 of page 3 in the specification applicants have defined the term "test pattern" as being, in essence, a time sequence of input signal vectors with an associated sequence of output signal vectors. The examiner cites Kurosaka's teaching of an intermediate format data file 106 as anticipating a pattern profile that represents a test pattern. However, Kurosaka does not here or elsewhere teach

or suggest the quoted element. To the contrary, Kurosaka teaches "The data file 106 in the intermediate format ... is provided ... to store detailed circuit information". Col. 7, lines 6-9. Kurosaka uses this file to store circuit information for two circuits that he wishes to compare using a point-detection algorithm. Col. 7, lines 12-16. No sequence of input signal vectors is represented by data file 106.

McNamara teaches a test generator that constructs a set of test vectors from a circuit design coded in a circuit design language. Col. 3, lines 22-43. The test generator interprets the circuit design as a series of blocks connected by transition arcs to form a state diagram, and constructs a first set of test vectors to cause each block to be visited and each transition arc to be taken. A second set of test vectors is also constructed to ensure user-selected transition paths are taken. Col. 4, lines 28-37. As with Kurosaka, the data structures represent the circuit design, and not a test pattern. The examiner cites, and applicants find, no teaching or suggestion of a test pattern profile in McNamara.

Valind teaches an automatic test pattern generator 56 that operates on a detailed circuit description 54 to generate test patterns. Fig. 4. The test pattern generator uses logic cone tracing and partitioning of the circuit logic to generate scan vectors that will detect stuck-at-1 and stuck-at-0 faults. Col. 9, lines 15-50. The examiner cites the detailed circuit description 54 as anticipating applicant's claimed test pattern profile. However, as with Kurosaka and McNamara, the detailed circuit description and derivative data structures are used to represent the circuit design, and not a test pattern.

Independent claims 11 and 17 also recite test pattern profiles as required elements. Applicants respectfully submit that independent claims 1, 11 and 17, along with their dependent claims, are allowable over the cited art for at least the reasons given above.

Conclusion

Applicants submit that this response constitutes a complete response to all of the issues raised in the Office Action dated June 20, 2002. Applicants have responded to the various

rejections under 35 U.S.C. § 102(e) and 103(a). In view of the foregoing amendments and remarks, applicants submit that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited.

In the course of the foregoing discussions, applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

If any fees are inadvertently omitted or if any additional fees are required or have been overpaid, please appropriately charge or credit those fees to LSI Logic Deposit Account Number 12-2252/P-3270/DJK.

Respectfully submitted,

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